The cited reference is indeed closely related art and relates to a debugger interface for a reduced instruction set signal processor. In particular, the cited reference is concerned with an encoding scheme whereby some limited information regarding a 24-bit datum can be expressed as an 8-bit datum. The claimed invention is different and non-obvious for several reasons described in detail below. In general, the present invention is concerned with providing a real time debugging interface for an embedded system which may contain several processors on a single chip. It is an important object of the invention to provide a real time debugger interface which does not interfere with the operation of the processor(s) or system bus. It is also an important object that the debugger interface of the invention use the fewest number of pins possible while at the same time providing a substantial amount of information about the executed instructions.

With regard to claim 1, the Examiner has attempted to illustrate in Folwell et al. where each element of claim 1 is taught or suggested as being obvious. However, the Examiner's analysis appears to contain several errors.

First, the Examiner points out that Folwell et al. discloses a "program counter means" at col. 5, lines 4-5. However, no such program counter means can be found at those lines of the Folwell et al. disclosure. Even considering the entire first paragraph of

col. 5, i.e. lines 1-6, no program counter means is mentioned. These lines recite three different registers and three different buffers. A careful search of the text of Folwell et al. does show that the term "program counter" is mentioned several times. However, it is not identified in any of the figures and it is not identified as being "coupled to said instruction memory means for indexing said instructions" as required by claim 1.

Second, the Examiner has identified the "instruction decode 22" in Figure 2 of Folwell et al. as corresponding to the "first decoder means" claimed in rejected claim 1. Claim 1 requires that this decoder means be "coupled to said instruction memory means, said program counter means, and said cause register means, said first decoder means having a first output". The instruction decode 22 described by Folwell et al. has an output 26 but is otherwise only coupled to the instruction memory 21. As mentioned above, there is no clear disclosure by Folwell et al. of a program counter as being coupled to anything. The Examiner states that col. 1, line 62 through col. 2, line 4 discloses what is claimed in clause "d)" of claim 1. However, that text fails to teach or suggest that a decoder is coupled to a program counter or coupled to a cause register.

Finally, the Examiner states that Folwell et al. does not specifically teach a decoder which operates "in real time" as required by the last clause of claim 1. Nevertheless, the

Examiner states that it would have been obvious that the decoder described by Folwell et al. operates in real time. The Applicant does not understand what point the Examiner is making. It should be appreciated that when the Applicant states that the present invention (not just the decoder portion of the invention) operates in real time, it means that the operation of the processor is not interrupted or slowed down to collect debugging data. On the contrary, Folwell et al. specifically calls for stopping the execution of the program during certain debugging procedures.

> "Neither the wait or the break instruction, in Group D of Table 3, cause the program address to change when they are executed; but they do cause the program counter to stop. A wait instruction is similar to the halt instruction in that it is used to save power. The wait instruction causes the arithmetic core's clocks to stop (leaving phase 1 on); but the I/O unit clocks are left running. The debug port will capture the program address when a wait instruction is executed." Col. 4, lines 55-62 of Folwell et al.

For the foregoing reasons, it is respectfully submitted that claim 1 of the instant application is neither anticipated nor suggested by Folwell et al.

With regard to claim 11, the Examiner states that Folwell et al. does not disclose "plural elements within an embedded system". The Examiner further notes that Folwell et al. shows a SCSI interface in a workstation which couples via an interface module to the debug port of the signal processor system (RSP device 11). The Examiner opines that Folwell et al. obviously suggests that

plural elements could be coupled to the same workstation via the expandable SCSI bus. However, contrary to the Examiner's opinion, such a coupling would not result in "an embedded system having a plurality of processors" as claimed in claim 11. Rather, it would result in a plurality of RSP devices all coupled to the same workstation. Further, as argued above with respect to claim 1, Folwell et al. (1) fails to suggest the claimed program counter means coupled to instruction memory means, (2) fails to suggest the coupling of cause registers to processors, (3) fails to suggest first decoder means coupled to instruction memory means, program counter means, and cause register means, and (4) fails to provide information in real time.

With regard to claim 21, the Examiner refers to the Abstract of Folwell et al. for teaching that the debugger port operates in real time. As mentioned above with reference to claim 1, the Folwell et al. device does not operate in real time as contemplated by the present invention. Claim 21 has been amended to include the limitations of claim 22 which corresponds to claims 3 and 13. Thus, the argument offered below with respect to claims 3 and 13 apply to amended claim 21 as well.

With regard to claims 2, 12, and 24, these claims depend from claims 1, 11, and 21 respectively and the arguments made above regarding claims 1, 11, and 21 apply to these claims respectively.

As to claims 3 and 13, the Examiner states that col. 1, lines 34-36 of Folwell et al. teach that "said clock cycle is a processor clock cycle", and col. 1, lines 5-9 and 34-35 teach that "said first decoder means updates said information about each instruction executed by said processor for each said processor clock cycle."

Col. 1, lines 5-11 of Folwell et al. state:

> "This invention relates to a means of verifying program flow within an inaccessible computer processor. It is incorporated in a debug port built within the internal logic of a single-chip, reduced instruction set, signal processor called the RSP device. It is used instead of a logic analyzer, since the device's internal program address bus is not available at its interface."

Col. 1, lines 34-36 of Folwell et al. state:

> "This means that a great deal of the functional operation of the device is internal and therefore no longer available to external development tools."

Clearly, neither of these sections of Folwell et al. teach or suggest what is claimed in claims 3, 13, and 22. Folwell et al. actually teach to the contrary of claims 3, 13, and 22. According to Folwell et al., information is not updated about each instruction or for each processor cycle. Folwell et al. attempts to solve the bandwidth constraints of an 8-bit debug port by only sending information about certain discontinuities in program execution which occur at branches, subroutines, etc. As shown in

the Tables in the Folwell et al. disclosure, it is only these program instructions for which any information is collected. Thus, Folwell et al. fails to update information about each instruction since many instructions are not of the type considered to be "discontinuities". Similarly, Folwell et al. does not update for each processor cycle because many processor cycles are spent executing instructions which are not of the type considered to be "discontinuities". Claims 3 and 13 are also allowable for the reasons stated above with regard to claims 1 and 11.

Claims 4, 14, and 23 claim the limitation that "said information about each instruction executed by said processor includes an indication whether or not an instruction has been executed since a previous processor cycle." Since Folwell et al. does not update information for each instruction nor for each processor cycle, Folwell et al. cannot perform the function claimed in claims 4, 14, and 23. The Examiner states that col. 1, line 62 through col. 2, line 4 of Folwell et al. teach this feature. However, they teach quite the opposite.

> "The present invention solves this problem by taking advantage of the sequential characteristics of application programs. Since discontinuities occur in the count of the program address counter in only a limited number of situations (i.e. branches, jumps, subroutine calls, returns from subroutines, exceptions, returns from exceptions, traps, returns from traps, and loopbacks to the tops of loops), the debug port takes advantage of this fact and captures program flow data only when certain discontinuities occur. As a result, output data is greatly reduced." Col. 1, line 62 - Col. 2, line 4 of Folwell et al. [Emphasis added.]

Claims 4, 14, and 23 are also allowable for the reasons stated above with regard to claims 1, 11, and 21.

Claims 5 and 15 claim that the first output of the debugger is a "three-bit parallel output". While the Examiner logically argues that an 8-bit output includes a 3-bit output, the claims at issue did not state that the output comprises three bits. Rather, they stated that the output is a 3-bit output. Nevertheless, these claims have been amended to state that the output consists of a 3-bit output, thereby excluding outputs with more bits. Folwell et al. repeatedly restates that the 8-bit output is a challengingly small bandwidth. A fair reading of Folwell et al. would suggest to one of ordinary skill that to perform the same function using only a three bit output would require an act of invention. Further, as explained above, the present invention provides more useful information than that provided by Folwell et al. The Examiner's statement that the eight bit output of Folwell et al. "could have been designed to use three bits" begs the question of whether it would have been obvious. There is nothing in Folwell et al. to suggest that the output could or should have been three bits and the Examiner has offered no evidence to support what "could have been". Claims 5 and 15 are also allowable for the reasons stated above with regard to claims 1 and 11.

Claims 6 and 16 further include the limitations of a second decoder and an event history buffer. The event history buffer has a data input, a data output, and an enable input. The second decoder is coupled to the cause register and to the enable input of the history buffer. The cause register has a second output which is coupled to the data input of the history buffer. The decoder decodes the contents of the cause register and enables the history buffer to capture those contents for particular events.

The Examiner refers to col. 5, lines 8-27 and col. 7, line 60 through col. 8, line 11 of Folwell et al. as teaching the arrangement claimed in claims 6 and 16. Col. 5, lines 8-27 refer to the same PAB/PAC copy capture control logic referred to by the Examiner with reference to the first decoder claimed in claim 1. One element in the prior art cannot be used to negate two elements in the Applicant's claim. If this disclosure in Folwell et al. represents the Applicant's first decoder, it cannot also represent the event history buffer or the second decoder. Col. 7, line 60 through col. 8, line 11 of Folwell et al. describe a "command unit" which receives commands from either the programmer workstation or the debug port to enable/disable the program flow unit. The command unit "can also command the program flow unit to capture program addresses". None of this teaching meets or suggests that limitations of claims 6 or 16. Neither the command unit nor any of its associated units can be considered the claimed second decoder or the claimed history buffer. Claims 6 and 16 are

also allowable for the reasons stated above with regard to claims 1 and 11.

Claims 7, 17, and 25 specify that the second decoder enables the event history buffer when the contents of the cause register indicate an interrupt, an exception, or a jump. The Examiner refers to col. 1, line 64 - col. 2, line 3, and col. 8, lines 1-9 as teaching the limitations of these claims. The cited portion of cols. 1 and 2 refers to portions of Folwell et al. which the Examiner previously referred to as performing the function of the Applicant's first decoder. They cannot be used now to represent a different element of the Applicant's invention. The cited portion of col. 8 refers to the command unit described above with respect to claims 6 and 16. The debug port of Folwell et al. can receive commands from either the internal circuitry or from the workstation coupled to it in order to stop and step through programs. The Examiner is confusing features of the first and second decoder means and improperly attempting to read certain portions of the reference twice to mean different things at different times. Claims 7, 17, and 25 are also allowable for the reasons stated above with regard to claims 1, 11, and 21.

Claims 8 and 18 specify that the data output of the event history buffer is a bit serial output. The Examiner states that the output FIFO mentioned at col. 8, line 9 of Folwell et al. "could be configured to have a serial output". Again, it is

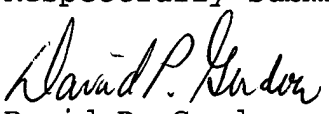
respectfully submitted that what could have been or might have been is not a substitute for evidence of obviousness. The fact that an invention is possible does not make it obvious. According to the present invention, parallel outputs are provided for the first decoders which output information about all program cycles. A single serial output is provided from the buffer which receives information about only some program cycles from the cause register as decided by the second decoders. Folwell et al. discloses a single eight bit parallel output which provides information about only some program cycles. The single eight bit port of Folwell et al. is actually functionally more similar to the Applicant's history buffer in terms of the kind of information it contains. Folwell et al. does not disclose any mechanism for achieving the functionality of the Applicant's first decoders' three bit outputs. Claims 8 and 18 are also allowable for the reasons stated above with regard to claims 1 and 11.

Claims 9, 10, 19 and 20 are also allowable for the reasons stated above with regard to claims 1 and 11. Moreover, Folwell et al. does not disclose anything analogous to the two types of outputs provided by the present invention, Folwell et al. only discloses a single parallel output.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is

invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,



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